IN THE CLAIMS:

Please cancel claims 21 and 34 without prejudice or disclaimer as to the subject matter contained therein.

Please amend the claims as shown in the following claims listing.

1-19. (Cancelled)

20. (Currently amended) A wireless communication device comprising:

~~a host processor and configured to execute instructions belonging to an instruction set of a first processor family; and~~

a single integrated circuit die including:

a reconfigurable processor core ~~coupled to the host processor, wherein the reconfigurable processor core includes~~ including a plurality of processors, wherein a first portion of the plurality of processors is configured to execute instructions belonging to an instruction set of a first processor family and wherein a second portion of the plurality of processors is configured to execute instructions belonging to an instruction set of a second processor family, wherein the second portion of the plurality of processors is coupled to memory locations storing instructions executable by the second portion to implement a set of host processor functionality that includes controlling portions of the reconfigurable processor core and interfacing with a system external to the wireless communication device ~~portions of the plurality of processors are selectably configurable to execute instructions belonging to a plurality of instruction sets~~;

a non-reconfigurable host processor coupled to the reconfigurable processor core and configured to execute instructions belonging to the instruction set of the first processor family, wherein the non-reconfigurable host processor is coupled to memory locations storing instructions executable by the non-

reconfigurable host processor to implement the set of host processor functionality; and

~~wherein a first portion of the plurality of processors is configured to execute instructions belonging to an instruction set of the first processor family;~~

~~wherein a second portion of the plurality of processors is configured to execute instructions belonging to an instruction set of a second processor family; and~~

a processor type select circuit configured to select either the non-reconfigurable host processor or the second portion of the plurality of processors to implement the set of host processor functionality.

~~wherein the host processor and the reconfigurable processor core are both located on a single integrated circuit die.~~

21. (Cancelled)

22. (Currently amended) The device as recited in claim [[21]], wherein the first portion of the plurality of processors is configured to execute instructions corresponding to signal processing functions while ~~processor type select circuit configured to selectably configure~~ the second portion of the plurality of processors executes the instructions stored in the memory locations that are executable to implement the set of host processor functionality ~~to execute instructions belonging to an instruction set of the first processor family subsequent to the second portion of the plurality of processors processing instructions belonging to an instruction set of the second processor family~~.

23. (Currently amended) The device as recited in claim 20, further comprising a plurality of digital signal processors configured to execute instructions corresponding to one or more embedded signal processing functions.

24. (Previously Presented) The device as recited in claim 20, wherein the second portion of the plurality of processors collectively forms a second host processor.

25. (Previously Presented) The device as recited in claim 20, further comprising an analog circuit portion located on the integrated circuit and coupled to a digital circuit portion that includes the host processor and the reconfigurable processor core, wherein the analog circuit portion includes:

a cellular radio core configured to provide two-way communication via one or more wireless channels;

a radio sniffer coupled to the cellular radio core; and

a short-range wireless transceiver core coupled to the cellular radio core and configured to provide two-way communication via one or more short-range wireless channels.

26. (Previously Presented) The device as recited in claim 25, wherein the reconfigurable processor core is coupled to the cellular radio core, and configured to process instructions corresponding to a plurality of wireless radio communication protocols.

27. (Previously Presented) The device as recited in claim 26, wherein the plurality of wireless radio communication protocols includes a Bluetooth™ or IEEE802.11 protocol.

28. (Previously Presented) The device as recited in claim 26, wherein the plurality of wireless radio communication protocols includes a Global System for Mobile Communications (GSM) protocol.

29. (Previously Presented) The device as recited in claim 26, wherein the plurality of wireless radio communication protocols includes a General Packet Radio Service (GPRS) protocol.

30. (Previously Presented) The device as recited in claim 26, wherein the plurality of wireless radio communication protocols includes an Enhance Data Rates for GSM Evolution (Edge) protocol.

31. (Previously Presented) The device as recited in claim 25, further comprising a router coupled to the host processor, the cellular radio core, and the short-range wireless transceiver core, wherein the router is configured to track destinations of packets and to send the packets in a parallel through a plurality of separate wireless communication channels.

32. (Previously Presented) The device as recited in claim 31, wherein the router is further configured to determine which of the plurality of separate wireless communication channels provides an optimum transmission medium, and to send the packets in a parallel in response to determining that more than one or more channels is less than optimum.

33. (Currently amended) A method comprising:

executing instructions belonging to an instruction set of a first processor family on a non-reconfigurable host processor of an integrated circuit die; [[and]]

storing instructions executable by the non-reconfigurable host processor to implement a set of host processor functionality;

~~selectably configuring portions of a plurality of processors of a reconfigurable processor core to execute instructions belonging to a plurality of instruction sets;~~

executing instructions belonging to [[an]] the instruction set of the first processor family on a first portion of a plurality of processor cores on the integrated circuit die;

executing instructions belonging to an instruction set of a second processor family on a second portion of the plurality of processor cores on the integrated circuit die;

storing instructions executable by the second portion of the plurality of processor cores to implement the set of host processor functionality; and

selecting either the non-reconfigurable host processor or the second portion of the plurality of processors to implement the set of host processor functionality.

~~locating the host processor and the reconfigurable processor core on a single integrated circuit die.~~

34. (Cancelled)

35. (Currently amended) The method as recited in claim [[34]] 33, further comprising ~~selectably configuring~~ the first portion of the plurality of processors executing instructions corresponding to signal processing functions while the second portion of the plurality of processors executes instructions to implement the set of host processor functionality ~~to execute instructions belonging to an instruction set of the first processor family subsequent to the second portion of the plurality of processors processing instructions belonging to an instruction set of the second processor family~~.

36. (Previously Presented) The method as recited in claim 33, processing instructions corresponding to a plurality of wireless communication protocols on the reconfigurable processor core.

37. (Previously Presented) The method as recited in claim 36, wherein the plurality of wireless communication protocols includes a Bluetooth™ or IEEE802.11 protocol.

38. (Previously Presented) The method as recited in claim 36, wherein the plurality of wireless communication protocols includes a Global System for Mobile Communications (GSM) protocol.

39. (Previously Presented) The method as recited in claim 33, further comprising:

determining which of a plurality of separate wireless communication channels of the plurality of wireless communication protocols provides an optimum transmission medium;

tracking destinations of packets and sending the packets in parallel through a plurality of separate wireless communication channels in response to

determining that more than one wireless communication channel is less than optimum.

40. (Currently amended) A communication system comprising:

a system host processor; and

a wireless communication device coupled to the system host processor and configured to provide wireless communication using a plurality of wireless communication protocols;

wherein the wireless communication device comprises:

~~a wireless host processor located on an integrated circuit die and configured to execute instructions belonging to an instruction set of a first processor family; and~~

a single integrated circuit die including:

a reconfigurable processor core coupled to the memory and ~~fabricated on the integrated circuit and coupled to the wireless host processor, wherein the reconfigurable processor core includes~~ including a plurality of processors, wherein a first portion of the plurality of processors is configured to execute instructions belonging to an instruction set of a first processor family and wherein a second portion of the plurality of processors is configured to execute instructions belonging to an instruction set of a second processor family, wherein the second portion of the plurality of processors is coupled to memory locations storing instructions executable by the second portion to implement a set of host processor functionality that includes controlling portions of the reconfigurable processor core and interfacing with the system host processor~~portions of the plurality of processors are selectably configurable to execute instructions belonging to a plurality of instruction sets~~;

a non-reconfigurable host processor coupled to the reconfigurable processor core and configured to execute instructions belonging to an instruction set of a first processor family, wherein the non-

reconfigurable host processor is coupled to memory locations storing instructions executable by the non-reconfigurable host processor to implement the set of host processor functionality; and

~~wherein a first portion of the plurality of processors is configured to execute instructions belonging to an instruction set of the first processor family;~~

~~wherein a second portion of the plurality of processors is configured to execute instructions belonging to an instruction set of a second processor family;~~ and

a processor type select circuit configured to select either the non-reconfigurable host processor or the second portion of the plurality of processors implement the set of host processor functionality.

~~wherein the host processor and the reconfigurable processor core are both located on a single integrated circuit die.~~

41. (New) The device as recited in claim 20, wherein the second portion of the plurality of processors is further configured to execute instructions corresponding to signal processing functions while the first portion of the plurality of processors executes instructions corresponding to signal processing functions.

42. (New) The method as recited in clam 33, further comprising the second portion of the plurality of processors executing instructions corresponding to signal processing function while the first portion of the plurality of processors executes instructions corresponding to signal processing functions.